

[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [Gmail](#) [more ▾](#)

[Sign in](#)

Google

"read port" "write port"

Search

[Advanced Search](#)
[Preferences](#)

New! [View and manage your web history](#)

Web

Results 1 - 10 of about 68,500 for "[read port](#)" "[write port](#)". (0.09 seconds)

Dual port memory with synchronized read and write pointers - US ...

a write logic circuit operationally coupled with the **write port** and the **read port** wherein the write logic circuit is configured to generate a FIFO full ...

www.patentstorm.us/patents/6166963-claims.html - 22k - [Cached](#) - [Similar pages](#)

Random access memory having independent **read port** and **write port** ...

Random access memory having independent **read port** and **write port** and process for writing to and reading from the same - US Patent 6262936 from Patent Storm.

www.patentstorm.us/patents/6262936.html - 17k - [Cached](#) - [Similar pages](#)

[[More results from www.patentstorm.us](#)]

Random access memory having independent **read port** and **write port** ...

A random access memory with a **read port**, a **write port**, a read/write control signal configured to control data transfer operations at the **read port** and/or ...

www.freepatentsonline.com/6445645.html - 54k - [Cached](#) - [Similar pages](#)

Altering Terminal Deficefiles

The code fragment presented in Figure 3-7 "Opening a **Read Port** and a **Write Port**" shows how a series of FCONTROL calls may be used to perform various device ...

docs.hp.com/en/32022-90052/ch03s04.html - 38k - [Cached](#) - [Similar pages](#)

FTC_LOADA.BAS 01-JAN-1999 Version 1.0 == Modified from Motorola ...

```
jbyte) fprintf(stderr,"Error writing first bank byte, got %d\n",jbyte); write(port,&bank,1); if ( (n = read(port,&jbyte,1)) <0) perror("Writing second ...
```

www.eol.ucar.edu/homes/onclely/PMB-doc/ftc.c - 6k - [Cached](#) - [Similar pages](#)

[PDF] [DDR/DDR2 Multi-channel Memory Controller](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

N x **Read port**. M x **Write port**. Command Arbiter. SD Control Core. DDR IO. The controller must be configured ... one **read port** and one **write port**. There is no ...

www.digidescorp.com/products/IP/DataSheets/DDC_DDR_datasheet.pdf - [Similar pages](#)

[PDF] [Memory - Synchronous RAMs](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

DW_ram_2r_w_s_dff Synchronous **Write-Port**, Asynchronous Dual **Read-Port** RAM ...

DW_ram_2r_w_a_lat **Write-Port**, Dual-**Read-Port** RAM (Latch-Based) ...

www.synopsys.com/products/designware/docs/doc/dwf/datasheets/syncram_overview.pdf -

[Similar pages](#)

ARM Interface Data Sheet

For instance, the Bluetooth interface block takes two ports: one **write port** for control and one **read port** for status. If you use the Bluetooth block, ...

bwrc.eecs.berkeley.edu/Research/Pico_Radio/

Test_Bed/Workspace/Xilinx_Library_pages/ARMIF_data_sheet.htm - 13k -

[Cached](#) - [Similar pages](#)

Write and read remote device PCI registers

Write port. **Read port**. Size. NcRpci_WritePortUlong · NcRpci_ReadPortUlong. ULONG. NcRpci_WritePortUshort · NcRpci_ReadPortUshort. USHORT ...

www.plxtech.com/.../Write_and_read_remote_device_PCI_registers.htm - 20k -

[Cached](#) - [Similar pages](#)

[PDF] [ISSCC 2005 / SESSION 20 / PROCESSOR BUILDING BLOCKS / 20.6](#)

File Format: PDF/Adobe Acrobat

A 32b 64-Word 9-**Read-Port**/7-**Write-Port**. Pseudo Dual-Bank Register File Using. Copied
Memory Cells for a Multi-Threaded. Processor ...

ieeexplore.ieee.org/iel5/9995/32118/01494030.pdf - [Similar pages](#)

[1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) **[Next](#)**

Try [Google Desktop](#): search your computer as easily as you search the web.

"read port" "write port"

[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)

©2007 Google - [Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)